20.6 A 0.9V 2.6mW Body-Coupled Scalable PHY Transceiver for Body Sensor Applications

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Physiological signals such as body temperature, heart rates and electrocardiogram (ECG) have been widely utilized for health monitoring applications. In order to detect the signals without cumbersome wires, heterogeneous body sensor nodes including wearable or implantable biomedical devices are wirelessly connected to each other forming a personal body sensor network (BSN) [1]. The physiological signals show different bandwidth and require various transmission rates [2]. Therefore, each sensor node needs a low power and scalable wireless transceiver running at the pertinent data rates for energy-efficient transmission. A wideband signaling transceiver for body-coupled communications (BCC) was proposed in [1] for such applications. However, since the previously reported transceiver had a fixed data rate of 2Mb/s without any modulation, it is not suitable for BSNs over the shared body channel. This paper presents a low power and scalable PHY transceiver integrated with an energy-efficient baseband processing unit. It enables packet-based data communications between the sensor nodes over the shared body channel.

Figure 20.6.1 shows the overall system block diagram and the proposed PHY packet format. Since the PHY transceiver adopts the wideband signaling scheme presented in [1], the node uses only a single electrode for transmitting and receiving the sensor data. The PHY transceiver adopts the direct sequence spread spectrum (DSSS) technique for both the fast code acquisition and the narrowband interference rejection because of its orthogonality and scalability properties. The analog front-end (AFE) accomplishes wideband amplification, digital conversion and 3-level pulse shaping for the pulse-position modulation (PPM) signals. The digital baseband (DBB) conducts pulse detection, pulse position synchronization and modulation/demodulation, code acquisition and scalable clock and data recovery (CDR). According to the investigation of the human body characteristics in [1] and [3], the shared body channel has no multi-path effect and no spreading delay. Since each sensor node is stationary on the body and the near-field electric coupling is the dominant mechanism in the link, the packet can be transferred with tolerable frequency drift over the channel. The frequency band for the 3-level PPM and DSSS is in the range of 10 to 70MHz suitable for BCC. Taking these characteristics of the body channel into consideration, the PHY packet format, as illustrated in Fig. 20.6.1, is designed to facilitate the realization of an energy-efficient receiver over and above that of RF-based receivers. The packet structure consists of four components: a synchronization (SYNC) header, a PHY header, a variable length payload and a cyclic redundancy check (CRC). The SYNC header is designed with two fields, a 4b preamble and 16b SYNC ID code. Particularly, the SYNC ID code is generated by XORing the 8b ID address of a sensor node and its complementary copy with a 16b orthogonal gold code (OGC), chosen as the spreading code providing perfect orthogonality [4]. This formation not only provides fast packet synchronization but also decreases detection time to accept the packet for a sensor node without despreading and recovering of the PHY header or payload data, thereby reducing packet reception energy of the PHY transceiver. Orthogonal variable spreading factor codes (OVSFC) are used as the channel code to spread the PHY header and payload data to the chip rate. It preserves orthogonality between the body channel with scalable data rates and the data spreading factor (DSF). For more scalability, the pulse separation factor (PSF) is used to vary the time interval between each pulse bit.

The AFE architecture is optimized with the circuit model for the body channel proposed in [3]. Like pulse-based UWB, it does not need the blocks related to carrier signals including mixers. With the supply voltage limited to 0.9V, it utilizes cascaded amplification, a feedback configuration for wide linearization and a time-interleaved ADC architecture as shown in Fig. 20.6.2. The ADC operating at the sampling clock of 160MHz consumes a large portion of the AFE power. To reduce the ADC power, the ADC incorporates two low power techniques: a pulse detector and cross-delayed sampling (CDS). The ADC is activated by the ADCEN signal generated from the pulse detector (only 70μW) only when pulse signals exist over the channel. However it suffers from lagging of the ADCEN signal due to the response time of the pulse detector. For this reason, the ADC employs a time interleaved architecture exploiting the CDS technique. It allows 3 half-clock delayed sampling as well as lower power dissipation for S/H circuits in the ADC. With the help of the pulse detector and the CDS technique, the power consumption of the ADC can decrease by 40%. The ADC resolution is chosen as 1b instead of 2b to reduce the circuit complexity and power consumption of the DBB.

Figure 20.6.3 shows the block diagram of the proposed DBB transceiver. The low power DBB is realized as a hierarchical block gating (HBG) architecture for energy-efficient packet processing from a 0.9V supply. According to the HBG scheme, each building block can be gated by controlling three ADCEN, PSYNC and IDSYNC signals. The demodulator, the matched filter (MF) and the OVSFC despreader are based on a parallel structure for scalability. The MF achieves fast code acquisition to reduce energy consumption. Since the physiological signals are digitally converted to regular pattern sequences [5], a parallel structure is chosen for the MF. The simulation results show a MF power reduction by 40% for the bit sequence with alternating signs. The proposed scalable OVSFC despreader is based on a scalable matched sense amplifier configuration that enables the despreader to recover the raw data as long as the spreading bit errors are less than 50%. In order to further reduce the power consumption of the DBB, a clock-gated D flip-flop (D-FF) with a master-slave structure for low-energy designs [6] is utilized in the high-speed blocks. Since clock skews increase at low supply voltage, a clock-skew insensitive C^2MOS D-FF is used in the low-speed blocks. The clock-gated D-FF reduces the power by about 30% for the parallel building blocks.

The proposed PHY transceiver is fabricated in 0.18μm standard CMOS and occupies an area of 2mm^2. All measurements are conducted by using a 25cm length phantom model composed of 0.9% NaCl physiological saline. Figure 20.6.4 shows the timing diagram and frequency spectrum of the TX output signal with 3-level PPM for the ECG sensor data at 1.25Mb/s (DSF=4, PSF=2) and the bottom shows the recovered ECG signals from the modulated TX output. Figure 20.6.5 shows measured bit error rates versus DSF and PSF for packet sizes of 512B. The chip performance summary is presented in Fig. 20.6.6. Figure 20.6.7 shows a micrograph of the transceiver chip. The reception bit energy of the transceiver chip is 0.19nJ/b, which is 50 times more efficient than the recently reported UWB receiver (9.6nJ/b) [7] for wearable and wireless body area networks.

References:

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[5] H. Kim, et al., "A Low Power 16-bit RISC with Lossless Compression Accelerator for Body Sensor Network System," *Proc. ASSCC,* pp. 207-210, Nov., 2006.

[6] D. Markovic, et al., "Methods for True Energy-Performance Optimization," *J. Solid State Circuits*, vol. 39, pp. 1282-1293, Aug., 2004.

[7] J. Ryckaert, et al., "A 16mA UWB 3-to-5GHz 20Mpulses/s Quadrature Analog Correlation Receiver in 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 114-115, Feb., 2006.

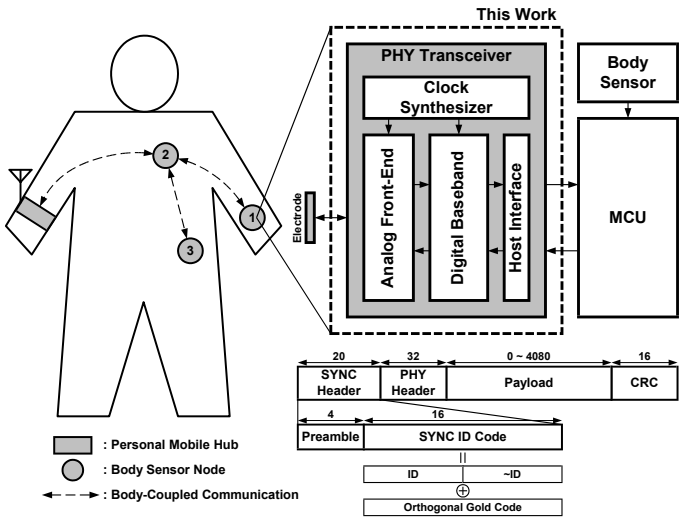

Figure 20.6.1: System block diagram and proposed physical layer packet format.

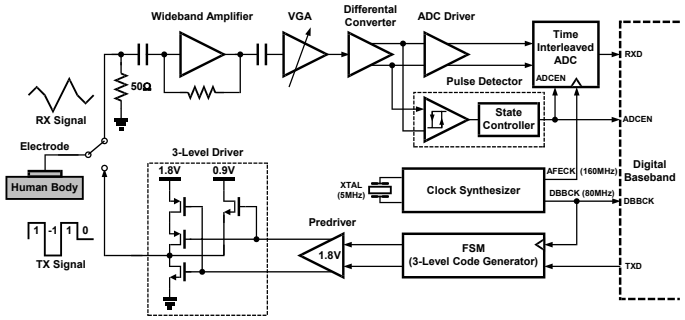

Figure 20.6.2: Proposed analog front-end architecture.

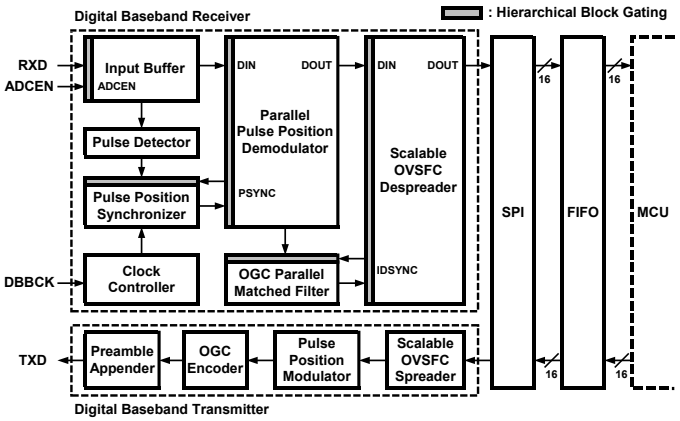

Figure 20.6.3: Block diagram of proposed digital baseband transceiver.

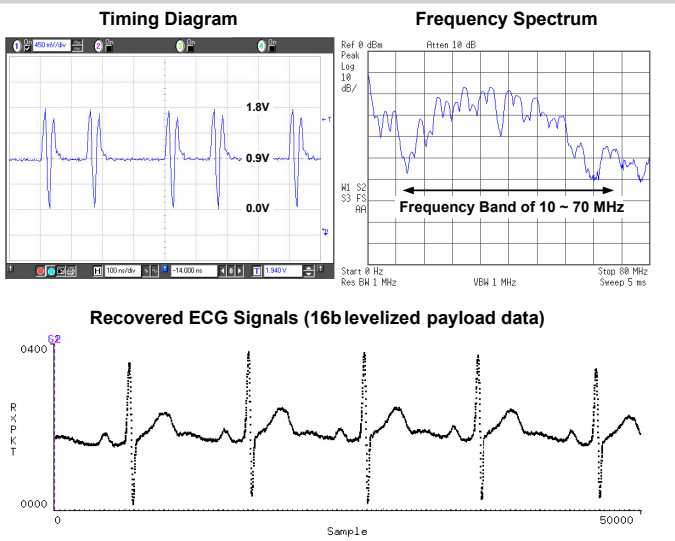

Figure 20.6.4: Measured timing diagram and frequency spectrum of TX output with 3-level PPM and recovered ECG signals at 1.25Mb/s.

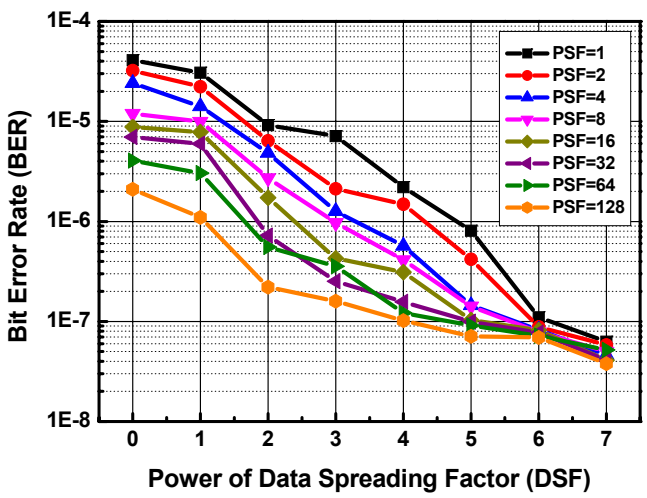

Figure 20.6.5: Measured bit error rates versus DSF and PSF for 512B packets.

Receiver Sensitivity		20 mV_{PP}
Voltage Gain		32 dB
Operating Bandwidth		6 ~ 120 MHz
Sampling Rate		160 MHz
Bit Interval		100 ns
Modulation		3-Level PPM + DSSS
Frequency Band		10 ~ 70 MHz
Synchronization Code		OGC ⊕ ID
Channel Spreading Code		OVSFC
Pulse Separation Factor (PSF)		2^0 ~ 2^7
Data Spreading Factor (DSF)		2^0 ~ 2^7
Data Rate		10 / (PSF x DSF) Mb/s
Chip Rate		10 / PSF Mchip/s
Code Acquisition Time		2 x PSF μs
Power Consumption	Analog Front-End	TX 0.52 mW / RX 1.38 mW
	Digital Baseband	TX 0.19 mW / RX 0.32 mW
	Clock Synthesizer	0.19 mW
	Overall	2.6 mW
Supply Voltage		Core 0.9 V & 1.8 V / IO 3.3 V
Core Area		1 x 2 mm^2
Technology		0.18μm Standard CMOS

Figure 20.6.6: Performance summary.

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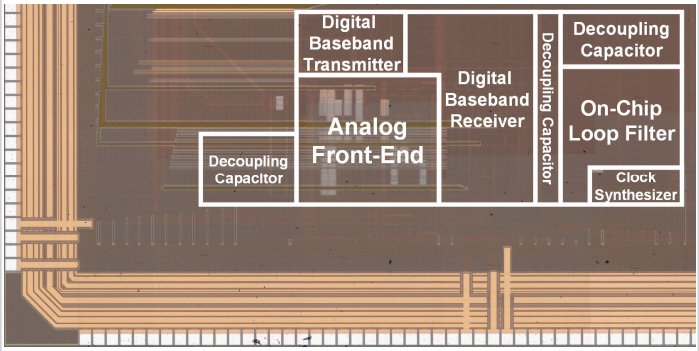

Figure 20.6.7: Chip micrograph.

